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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,855	KWA ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-28 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 December 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 28 are presented for the examination.

Specification

2. The disclosure is objected to because of the following informalities:

3. In the specifications, replace numerals "322" and "324" with ---332--- , and ---334--- respectively in line 3 of para 0030 on page 12 as numerals for side band signals are not matching with the figure's numerals.

4. The use of the trademark [PCI EXPRESS] has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner, which might adversely affect their validity as trademarks.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before

> the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 12, and 24 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Verdun, US patent application publication 2005/0044448 A1.

7. As to claim 1, Verdum discloses a method to manage power in a system [10, fig. 1], the method [para 0007 on page 1] comprising:

a. monitoring transactions [by racking write buffer] over an interconnect [PCI bus] coupling a chipset device [26 memory controller hub] and a peripheral device [inherent to computer system] in the system [10, fig. 1], the transactions being transmitted between the peripheral device and the chipset device [via PCI bus] according to a flow control protocol that allows the chipset device [26] to keep track of the transactions [para 007 on page 1, para 0015 – 0018 on page 2]; and

b. causing a processor [12] in the system [10] to exit from a power state [low power state] if a plurality of coherent transactions pending in a buffer of the chipset device [26] exceeds a first threshold [buffer is full] [para 0019 - 0021 on page 2 – 3, fig. 1, 3].

8. As to claim 12, Verdum discloses an apparatus in a computing system, the apparatus comprising:

a. power management circuitry to monitor transactions [by racking write buffer] over an interconnect coupling a root complex device [18] and a peripheral device [inherent to computer system] in the system [10, fig. 1], in the computing system [10], the transactions being transmitted between the

peripheral device [inherent to computer system] and the root complex device [18] according to a flow control protocol [inherent to write tracking] to allow the root complex device [18] to keep track of the transactions transmitted [para 007 on page 1, para 0015 – 0018 on page 2]; and

b. a digital media interface [bus interconnect] coupled to the root complex device [18] to send a first message packet to the root complex device to cause a processor [12] in the computing system [10] to exit from a power state [low power state] if a plurality of coherent transactions pending in a buffer of the root complex device [18] exceeds [reached] a first threshold [buffer full] [para 0019 - 0021 on page 2 – 3, fig. 1, 3].

9. As to claim 22, Verdum discloses a system [10, fig. 1] comprising:

a. a processor [12];

b. a memory controller [18] coupled to the processor [12];

c. a graphics chip [20];

d. an interconnect [bus] coupling the graphics chip [20] to the memory controller [18] [shown in fig. 1];

e. an input/output controller [24], coupled to the memory controller [18], comprising

(i) power management circuitry to monitor transactions over the interconnect, the transactions being transmitted between the graphics chip [20] and the memory controller [18] according to a flow control protocol; and

(ii) a digital media interface [bus interconnect] coupled to the memory controller to send a first message packet to the memory controller to cause the

processor to exit from a power state if a plurality of coherent transactions pending in a buffer of the memory controller exceeds [reached] a first threshold [buffer full] [para 007 on page 1, para 0015 – 0018 on page 2, para 0019 - 0021 on page 2 – 3, fig. 1, 3].

10. Claims 1 – 17, and 24 – 28 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Yavatkar et al. [hereinafter as Yavatkar], US patent application publication 2003/0137945A1.

11. As to claim 1, Yavatkar discloses a method to manage power [energy usage] in a system [fig. 1], the method [para 0002 – 0005, 0014 on page 1] comprising:

a. monitoring [by examining] transactions [buffer capacity] over an interconnect [network] coupling a chipset device and a peripheral device [inherent to handheld computers, wireless devices, or embedded devices] in the system [para 0008 on page 1], the transactions being transmitted between the peripheral device and the chipset device according to a flow control protocol [TCP transmission control protocol] that allows the chipset device to keep track of the transactions [para 0018 – 0019 on page 2, fig. 1 – 2]; and

b. causing a processor in the system [fig. 1] to exit [wake up] from a power state [low power state] if a plurality of coherent transactions pending in a buffer of the chipset device exceeds [reached] a first threshold [maximum capacity threshold] [para 0017 - 0019 on page 2, fig. 4].

12. As to claim 12, Yavatkar discloses an apparatus in a computing system [fig. 1], the apparatus comprising:

a. power management circuitry to monitor transactions [by examining buffer capacity] over an interconnect [network] coupling a root complex device and a peripheral device in the system [inherent to handheld computers, wireless devices, or embedded devices], in the computing system [para 0008 on page 1], the transactions being transmitted [inherent to network coupled system, fig.1] between the peripheral device and the root complex device according to a flow control protocol [TCP transmission control protocol] to allow the root complex device to keep track of the transactions transmitted {[para 0002 – 0005, 0014 on page 1, para 0018 – 0019 on page 2, fig. 1 – 2]; and

b. a digital media interface [inherent to network coupled] coupled to the root complex device to send a first message packet to the root complex device to cause a processor in the computing system to exit [wake up] from a power state [low power state] if a plurality of coherent transactions pending in a buffer of the root complex device exceeds [reached] a first threshold [maximum capacity threshold] [para 0017 - 0019 on page 2, fig. 4].

13. As to claim 22, Yavatkar discloses a system [fig. 1] comprising:

a. a processor [inherent to handheld computers, wireless devices, or embedded devices, para 0008 on page 1];

b. a memory controller coupled to the processor [inherent to handheld computers, wireless devices, or embedded devices, para 0008 on page 1];

c. a graphics chip [inherent to handheld computers, wireless devices, or embedded devices, para 0008 on page 1];

d. an interconnect [bus] coupling the graphics chip to the memory controller [inherent to handheld computers, wireless devices, or embedded devices, para 0008 on page 1];

e. an input/output controller, coupled to the memory controller [inherent to handheld computers, wireless devices, or embedded devices, para 0008 on page 1], comprising

(i) power management circuitry to monitor transactions over the interconnect [para 0002 – 0005, 0014 on page 1], the transactions being transmitted between the graphics chip and the memory controller according to a flow control protocol [TCP transmission control protocol, para 0018 – 0019 on page 2, fig. 1 – 2]; and

(ii) a digital media interface [bus interconnect] coupled to the memory controller to send a first message packet to the memory controller to cause the processor to exit [wake up] from a power state [low power state] if a plurality of coherent transactions pending in a buffer of the memory controller exceeds [reached] a first threshold [maximum capacity threshold] [para 0017 - 0019 on page 2, fig. 4].

14. As to claim 2, Yavatkar teaches managing power [energy usage] including timers to determine whether a predetermined period of time has passed if the plurality of coherent transactions pending in the buffer does not exceed the first threshold; and causing the processor to exit from the power state if the predetermined period of time has passed [timer to determine transmission is complete, step 330 in fig. 3, and 460 in fig. 4] [para 0018 on page 2, fig. 3].

15. As to claims 3 – 4, 13 – 14, and 25 – 26, Yavatkar teaches transmitter state protocol and receiver protocol state machine including entering processor into low power state and exiting [wake up] state with respect to first [low water mark] and second threshold [high water mark] including asserting and de-asserting indicator too [para 0017 – 0018 on page 1].

16. As to claims 5, and 15, Yavatkar teaches transmitter state protocol and receiver protocol state machine including entering processor into low power state and exiting [wake up] state with respect to first [low water mark] and second threshold [high water mark] and timers including determining predetermined period of time has passed and asserting and de-asserting indicator too [para 0017 – 0018 on page 1].

17. As to claims 6 – 8, 16, and 27, Yavatkar teaches transmitter state protocol machine and receiver protocol state machine including entering processor into low power state and exiting [wake up] state with respect to first [low water mark] and second threshold [high water mark] including first, and second threshold values and first threshold be substantially equal, lower and higher than the second threshold [para 0017 – 0018 on page 1].

18. As to claims 9, 17, and 28, Yavatkar discloses flow control protocols [TCP, IP, OSI], media access controller [MAC, 260] and data link layer [layer 2] defines topology control protocol for LAN specifications including peripheral component express [PCI EXPRESS][para 0019 – 0021 on page 2].

19. As to claims 10 – 11, Yavatkar discloses handheld computers, wireless devices, or embedded devices [para 0008 on page 1], which inherently teaches chip set devices including a memory controller, and an input/output controller.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

20. Claims 18 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilcox et al. [hereinafter as Wilcox], US Patent 6,820,169 B2, and further in view of Yavatkar et al. [hereinafter as Yavatkar], US patent application publication 2003/0137945A1.

21. As to claim 18, Wilcox discloses a semiconductor chip [104, chipset fig. 1], the semiconductor chip [104] comprising: (i) a memory controller [106] coupled to a peripheral device [as shown in fig. 1] in the computing system [100, fig. 1]; (ii) power management circuitry [314, power state control circuit, fig. 3] coupled to

the memory controller [106] to monitor [track] transactions between the peripheral device and the memory controller [106][fig. 3]; and (iii) an input/output controller [108] residing on a common substrate with the memory controller [as shown in fig. 1] to allow a processor [102] in the computing system [100] to control [enter/exit into/out] the power state [first/low, second/high power state] including suitable arbitration, buffering, and coherency management for each interface [col. 2, lines 17 – 19, 35 – 37, 43 – 56, col. 5, lines 11 – 59, col. 8, lines 44 – 67, col. 9, lines 1 – 12, fig. 1, 3].

However, Wilcox's power state control circuit does not teach to enter into a power state if a plurality of incoherent transactions pending in a buffer of the memory controller exceeds an entry threshold and to prevent the processor from entering into the power state if the plurality of incoherent transactions is below the entry threshold.

Yavatkar discloses an apparatus and method for managing energy [power] usage of processor by implementing a transmitter and receiver protocol state machine including enter into a power sate [wake up state] if a plurality of incoherent transactions pending in a buffer of the memory controller exceeds [reached] an entry threshold [low water mark][para 0017 on page 2] and to prevent [from waking] the processor from entering [stays in low power state] into the power state [low power state] if the plurality of incoherent transactions is below the entry threshold [maximum capacity threshold] [para 0018 on page 2, fig. 4].

It would have been obvious to one of ordinary skill in art, having the teachings of Wilcox and Yavatkar before him at the time of invention was made, to modify the control logic of power state control circuit of chipset as disclosed by Wilcox by implementing a transmitter and a receiver protocol state machine to control entry and exit of power state by monitoring transactions pending in a buffer with respect to a threshold as taught by Yavatkar in order to obtain a system for managing and conserving energy usage by operating across multiple instances of a protocol state machine and across multiple layers of protocol in a layered architecture, one of ordinary skill in the art wanted to be motivated to conserve energy [power] on energy conscious devices and reduces overall energy [power] usage [para 0001, para 0008 on page 1].

22. As to claim 19, Yavatkar teaches the processor to exit [wake up] from the power state [low power state] if a plurality of coherent transactions pending in the buffer of the memory controller exceeds [reached] an exit threshold [maximum capacity threshold][step 430 in fig. 4].

23. As to claim 20, Yavatkar teaches transmitter state protocol machine and receiver protocol state machine including entering processor into low power state and exiting [wake up] state with respect to first [low water mark] and second threshold [high water mark] including first, and second threshold values and first threshold be substantially equal, lower and higher than the second threshold [para 0017 – 0018 on page 1].

24. As to claim 21, Yavatkar teaches transmitter state protocol machine and receiver protocol state machine including entering processor into low power state

and exiting [wake up] state with respect to first [low water mark] and second threshold [high water mark] including first, and second threshold values and first threshold be substantially equal, lower and higher than the second threshold [para 0017 – 0018 on page 1] which inherently includes adaptively modifiable threshold too.

25. As to claim 22, Yavatkar discloses flow control protocols [TCP, IP, OSI], media access controller [MAC, 260] and data link layer [layer 2] defines topology control protocol for LAN specifications including peripheral component express [PCI EXPRESS][para 0019 – 0021 on page 2].

26. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

27. **Prior Art not relied upon**: Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am - 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
April 28, 2006

THUAN N. DU
PRIMARY EXAMINER